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[Title Of The Invention]
ELEMENT JUNCTION STRUCTURE FOR SEMICONDUCTOR MOUNTING BOARD AND ITS MANUFACTURE

[Abstract]
PURPOSE: To provide a semiconductor device mounting board capable of being made with low cost and having an input and output pin of high strength and a junction of a lead in a semiconductor device to which LSI's such as a multi- layer wiring substrate, a semiconductor package, an insulation substrate using glass ceramic or the like are mounted.
CONSTITUTION: In an element junction pad on a semiconductor mounting board 1, an element junction pad structure provided in a thin film metallized part 3 inside a cavity 2 is structured and parts such as a Kovar pin 6 or the like are connected with solder or brazing material 4. Even the semiconductor mounting board 1 having a comparatively low mechanical strength such as low temperature sintered glass ceramic, etc., can be used, and the element junction pad is metallized with a thin film in the cavity, whereby it is possible to obtain a junction body comprising glass ceramic having low cost and high strength and an input and output part composed of a metal or a brazing material.7 Glass ceramic board

[Claim(s)]
[Claim 1]A low-temperature-sintering board, an output pin, or joining structure with a lead, and said output pin and a lead consist of metal or an alloy, Element joining structure for semiconductor mounting boards, wherein said low-temperature-sintering board has the independent cavity which has thin film metallizing on the side and the bottom and said thin film metallizing, an output pin, or a lead is connected by solder or wax material.
[Claim 2]A manufacturing method of joining structure for semiconductor mounting boards characterized by comprising the following.
A process of forming a thin film layer in the whole surface including inside of a cavity of a ceramic substrate which provided a cavity.
A process of removing a thin film layer of portions other than inside of a cavity by grinding the surface of a substrate.
A process of joining an output pin or a lead by solder or wax material by making a thin film layer in a cavity into metallizing.

[Detailed Description of the Invention]
[0001]
[Industrial Application]This invention relates to the joining structure of the semiconductor device which mounts LSI, such as an insulating substrate which used a multilayer interconnection board, a thick film multilayer board, a semiconductor package, and crystallized glass.
[0002]
[Description of the Prior Art]Generally the element joining pad of the ceramic substrate for

semiconductor mounting is formed of thick film metallizing. However, thick film metallizing was formed in low-temperature-sintering boards, such as a glass ceramic board, and when the output pin and lead which consist of metal or an alloy were joined by solder or wax material, it had the problem of producing metallizing peeling. Then, the element joining pad on the conventional low-temperature-sintering board is formed with the thin film in many cases. The example of composition of the zygote of the mounting board at the time of forming thin film metallizing on the conventional mounting board and the output pin which comprises metal is shown in drawing 5. When forming the metallized pad of a thin film conventionally. Whether a thin film is formed in a substrate by sputtering or vacuum evaporation via a metal mask after substrate polish. The thin film metallized pad was formed through photo lithography and an etching process after sputtering or vacuum evaporation after substrate polish. When a metal mask was used, process time was made comparatively few, but by the pattern of a narrow pitch, it had the problem of causing a short circuit, for the surroundings lump to between the substrate of sputtering particles, and a mask. When the process of photo lithography was used, compared with the case where process time forms thick film metallizing, it became remarkably long, and it had the problem which has caused cost escalation. Since the tensile stress produced also in the case where thin film metallizing is used, at the time of junction by solder or wax material concentrated on a metallizing end, metallizing peeling might be produced.

[0003]From a point of the miniaturization of a package, densification, closure nature, and the propagation characteristic of a signal. Although many structures of mounting an LSI chip in a cavity are reported to JP,62-4859,A, JP,58-74047,A, JP,58-111350,A, JP,4-24955,A, etc., If it sees from a point of bonding strength even if what provided the element joining pad in the independent cavity is not reported but the element itself is in a cavity, the existence of a cavity does not have a meaning at all.

[0004]

[Problem(s) to be Solved by the Invention]As stated above, it was impossible to have obtained a zygote with the output pin and lead which comprise low cost, and high intensity low-temperature-sintering board and metal in the metallizing structure and joining structure on a low-temperature-sintering board, especially a glass ceramic board.

[0005]The purpose of this invention is to remove such a conventional fault and to provide the joining structure which can apply the crystallized glass which has junction to an output pin and a lead that it is producible by low cost, and high intensity on the semiconductor device mounting board made into representation.

[0006]

[Means for Solving the Problem]Let this invention be an element joining pad which comprises a thin film pad of the side in a cavity which became independent about a pad, and the bottom in an element joining pad on a low-temperature-sintering board with which a semiconductor is mounted.

[0007]An example of composition of an element joining pad of this invention is shown in drawing 1. Although a glass ceramic board or a ceramic substrate is suitably used as a mounting board used by this invention, the presentation is not limited and is applied to an extensive material. It is not limited for a conductive material used for a substrate. Neither a presentation nor thickness nor a formation method is limited also for thin film metallizing, but sputtering, vacuum evaporation, electroless deposition, electrolytic plating, etc. are

chosen suitably. Shape or size of a cavity are not limited, either.
[0008]An example by which a package lead and an output pin are joined to an element joining pad of drawing 1, respectively was shown in drawing 2 and drawing 3. Construction material of what is joined, and shape are not limited. Although an Ag-Cu system eutectic alloy is preferred also about wax material and solder, An Au-Si system alloy, an Au-germanium system alloy, an Au-Cu system alloy, an aluminum-Si system alloy, a Cu-Zn system alloy, a nickel-Cr system alloy, a Mg-aluminum system alloy, a Sn-Pb system alloy, a Sn-Zn system alloy, a Sn-Ag system alloy, a Sn-Sb system alloy, a Cd-Zn system alloy, a Pb-Ag system alloy, A Cd-Ag system alloy, a Zn-aluminum system alloy, an Au-Sn system alloy, etc. may be sufficient, limitation is not carried out but a glass ceramic board should just be the temperature (about 1000 degrees C or less) which a conductive material of softening or a substrate does not dissolve. It is still more effective after junction to plate nickel/Au etc. to an element pad and a joined alloy, or metal from a point of junction nature in a post process, or anti-corrosiveness.
[0009]Since fillet end of a metallizing end of wax material in which a lot of stress which becomes the cavity side and is produced at the time of junction remains does not correspond with an end of metallizing according to this invention, Metallizing peeling produced in a zygote without the conventional independent cavity cannot get up, and a high intensity zygote can be obtained.
[0010]An example of element joining pad manufacture of drawing 1 was shown in drawing 4. After forming thin film metallizing in the whole surface of a substrate in which a cavity was beforehand provided at the time of manufacture, an element joining pad which comprises thin film metallizing in a cavity can be obtained by grinding a substrate face. According to this method, since it is possible to reduce substantially process time which forms thin film metallizing, low cost-ization is realizable.
[0011]
[Example]The example to which various the substrate to be used, thin film layer composition, wax material, and junction elements were changed hereafter is shown.
[0012](Example 1) A cavity 0.8 mm in diameter, and 0.5 mm in depth. After forming Cr/Cu thin film layer in the multilevel interconnection glass ceramic board which has in a 1.27-mm pitch, used Ag-Pd as the inner conductor, comprised borosilicate glass and alumina, and was calcinated at 900 degrees C by sputtering by a thickness of 0.1 micrometer and 0.5 micrometer, respectively, The element joining pad in a cavity was formed by grinding a substrate face. The Ni thin film layer was formed by electroless deposition by a thickness of 0.1 micrometer on this pad, and the lead part which comprises the covar by which Au plating of the package made from 460 degrees C- alumina was carried out with Sn-Pb system solder was joined at 230 degrees C among nitrogen. Firm junction was acquired without causing destruction of peeling of a joined part etc., even if this package is vertical and it performs hauling of 10kgf in the direction of 45 degree. The process time which junction took was 50 minutes.
[0013](Example 2) After forming a Ti/Mo thin film layer in the same Ag-Pd multilevel interconnection glass ceramic board as Example 1 which has a cavity 1.7 mm in diameter, and 0.5 mm in depth in a 2.54-mm pitch by sputtering by a thickness of 0.1 micrometer and 1.5 micrometers, respectively, The element joining pad in a cavity was formed by grinding a substrate face. The Ni thin film layer was formed by electroless deposition by a thickness of 0.1 micrometer on this pad, and the output pin made from covar was joined at

780 degrees C among nitrogen by Ag-Cu system eutectic crystal wax material. The bonding strength of the output pin was perpendicular and showed 6.6kgf and sufficient value in 10 or more kgf and the direction of 45 degree. The process time which junction took was 1 hour.

[0014](Example 3) The Cr/Pd thin film layer was formed in the same Ag-Pd multilevel interconnection glass ceramic board as Example 1 which has a cavity 1.3 mm in diameter, and 0.5 mm in depth in a 2.54-mm pitch by sputtering by a thickness of 0.1 micrometer and 0.6 micrometer, respectively. Next, the element joining pad in a cavity was formed by grinding a substrate face. The output pin made from covar which performed Au plating with Au-Sn system solder was joined at 320 degrees C among nitrogen. The bonding strength of the output pin was perpendicular and showed 2.3kgf and a practical use possible value in 5kgf and the direction of 45 degree. The process time which junction took was 1 hour.

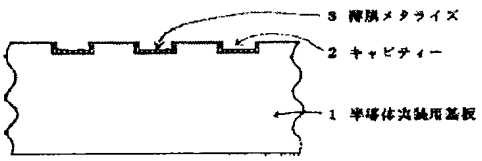
[0015](Comparative example 1) After grinding the surface of the same multilevel interconnection glass ceramic board as Example 1 without a cavity, After forming Cr/Cu thin film layer by sputtering by a thickness of 0.1 micrometer and 0.5 micrometer, respectively, patterning by photo lithography was performed and the with 0.8 mm in diameter of a substrate face and a pitch of 1.27 mm element joining pad was formed by wet etching. The Ni thin film layer was formed by electroless deposition by a thickness of 0.1 micrometer on this pad, and the lead part of other packages made from 460 degrees C-alumina was joined at 230 degrees C among nitrogen with Sn-Pb system solder. Even if this package was vertical and it performed hauling of 10kgf in the direction of 45 degree, the whole package did not separate. However, when hauling of 10kgf was performed in the direction of 45 degree, the lead of 23 had separated from the substrate side. The process time which junction took has become long with 1 hour and 30 minutes.

[0016](Comparative example 2) After grinding the surface of the same multilevel interconnection glass ceramic board as Example 2 without a cavity, After forming the thin film layer of Ti/Mo by sputtering by a thickness of 0.1 micrometer and 1.5 micrometers, respectively, patterning by photo lithography was performed and the with 1.7 mm in diameter of a substrate face and a pitch of 2.54 mm element joining pad was formed by wet etching. The Ni thin film layer was formed by electroless deposition by a thickness of 0.1 micrometer on this pad, and the output pin made from covar was joined at 780 degrees C among nitrogen by Ag-Cu system eutectic crystal wax material. Although the bonding strength of the output pin was perpendicular and showed 4.2kgf and a practical use possible value in 8.8kgf and the direction of 45, it was low intensity as compared with this invention. The process time which junction took has become long with 1 hour and 40 minutes.

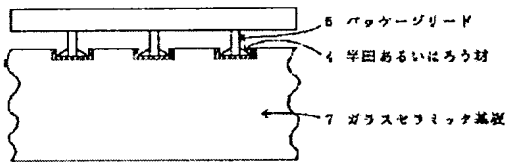
[0017](Comparative example 3) After grinding the surface of the same multilevel interconnection glass ceramic board as Example 3 without a cavity, After forming a Cr/Pd thin film layer by sputtering by a thickness of 0.1 micrometer and 0.6 micrometer, respectively, patterning by photo lithography was performed and the with 1.3 mm in diameter of a substrate face and a pitch of 2.54 mm element joining pad was formed by wet etching. The output pin made from covar which furthermore performed Au plating with Au-Sn system solder was joined at 320 degrees C among nitrogen. The bonding strength of the output pin was perpendicular and showed 1.7kgf and a low value in 4.3kgf and the direction of 45 degree. The process time which junction took has become long

with 1 hour and 40 minutes.
[0018]
[Effect of the Invention]As explained above, according to this invention, a zygote with the output pin and covar which comprise a low-temperature-sintering board, metal, or alloys including a high intensity glass ceramic board can be obtained. Since the process time which forms an element joining pad can be shortened, cost can be reduced.
[0019]The joining structure for semiconductor mounting boards by this invention is useful as joining structure of the semiconductor device which mounts LSI, such as an insulating substrate, a multilayer interconnection board, and a semiconductor package, and the industrial value is very high.
[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the structure of the joining pad of this invention.
[Drawing 2]It is a figure showing the joining structure of the substrate of this invention, and a package lead.
[Drawing 3]It is a figure showing the joining structure of the output pin to the substrate of this invention.
[Drawing 4]It is a figure showing the joining pad manufacturing method of this invention.
[Drawing 5]It is a figure showing the structure of the conventional joining pad.
[Description of Notations]
1 The substrate for semiconductor mounting
2 Cavity
3 Thin film metallizing
4 Solder or wax material
5 Package lead
6 Covar pin

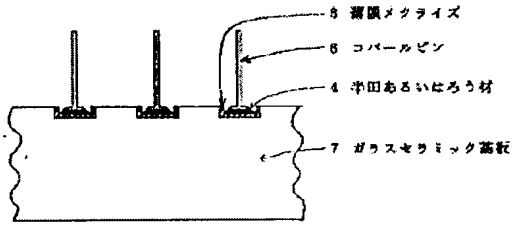
【図１】


3 薄膜メタライズ
2 キャビティー
1 半導体実装用基板

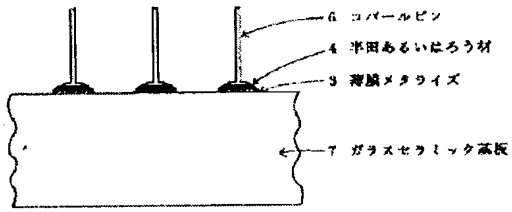
【図２】


5 パッケージリード
4 半田あるいはろう材
7 ガラスセラミック基板

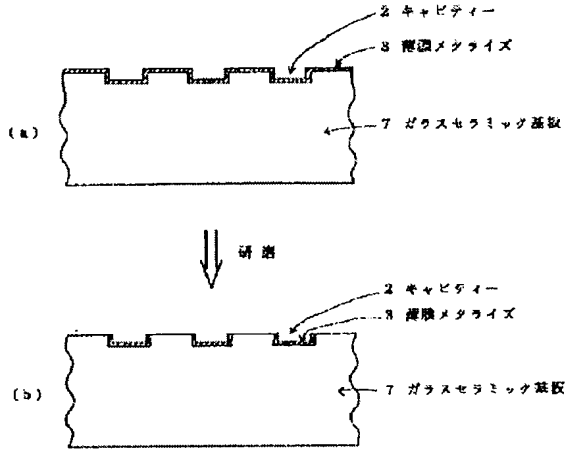
【図３】


3 薄膜メタライズ
6 コバールピン
4 半田あるいはろう材
7 ガラスセラミック基板

【図５】


6 コバールピン
4 半田あるいはろう材
3 薄膜メタライズ
7 ガラスセラミック基板

【図１】


2 キャビティー
3 薄膜メタライズ
(a)
7 ガラスセラミック基板
研磨
2 キャビティー
3 薄膜メタライズ
(b)
7 ガラスセラミック基板